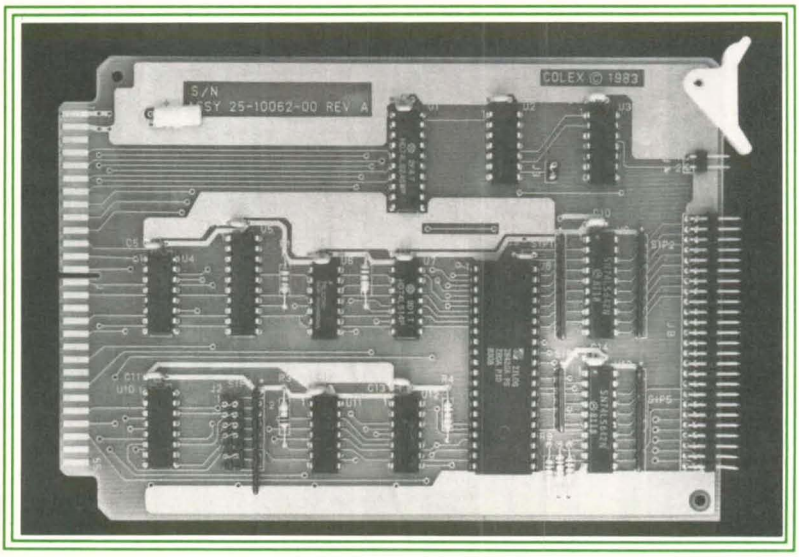
COLEX™

STD-SASI1

STD BUS



FEATURES

- □ STD-Z80 Bus Compatible
- □ 4 MHz Operation
- □ Supports Shugart Associates Systems Interface (SASI)
- □ Auto Handshake Logic
- □ Polled or Interrupt Driven
- □ I/O Addressing on 4 Byte Boundary
- □ IOEXP Supported
- □ +5 Volt only
- □ 1 year warranty

DESCRIPTION

The Colex STD-SASI1 is designed to interface to the Shugart Associates System Interface™. This interface is designed to allow users at a system level to connect mass storage peripherals without affecing software. The STD-SASI1 implements the host adapter on the STD Bus. This interface is the standard for Winchester 5¼ inch disk subsystems. The STD-SASI1 can operate in either a polled or interrupt transfer mode.

The STD-SASI1 consists of two major parts, a parallel data port and auto handshaking logic. This port is designed with a 3881 PIO chip. Port A is designated for data and will accept bi-directional information transfers. Port B is designated for status and control. The status signals are inputs, the control signals are outputs from the port. All signals are fully buffered to and from the PIO.

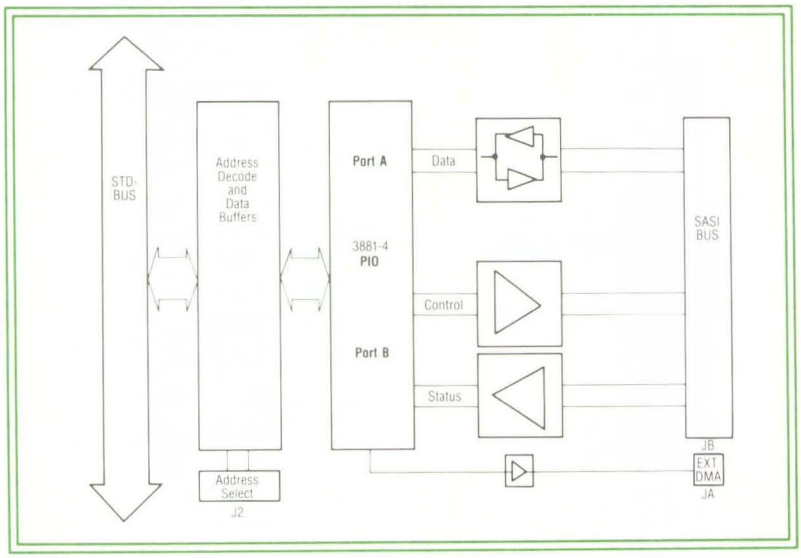
The STD-SASI1 will fully support Z-80 mode 2 interrupts as well as polled operation. The board also has an external connector JA allowing DMA operation. A twisted pair wire can be run from JA to the Colex STD-FLP2 card. The output signals an external READY output from this card. Both commands, data and status may be DMA'd to or from the STD-SASI1.

Automatic handshaking is supported. Jumper J3 enables a circuit that asserts the SASI ACK (acknowledge) signal after reading or writing to the SASI Bus. This provides an increase in throughput since software does not have to toggle the ACK control line.

™Trademark of Shugart Associates

COLEX AMERICA, INC. P.O. Box 801462, Dallas, Texas 75380, United States 214/458-2779
COLEX U.K., LTD. Index House, Ascot Berks, SL57EU, England, (0990)-23377
COLEX ASIA PACIFIC Luk Hop Industrial Bldg., 15th Floor, 8 Luk Hop St., San Po Kong, Kowloon, Hong Kong 3/7265651

STD-SASI1 BLOCK DIAGRAM



SPECIFICATIONS

ELECTRICAL

- System clock: 4.0 MHz
- Data bus: 8 bits, bi-directional
- Address bus: 16 bits
- Signal Loading: Inputs: One 74LS maximum
  Outputs: −3mA min @ 2.4 volts
  24mA min @ 0.5 volts
- Operating Temperature: 0°C to 60°C
- System Interrupt Units: 1 SIU
- Interrupts: All three Z80 modes
- Power Requirements:

Parameter	Condition	Min.	Typ.	Max.	Units
V_{CC}	—	4.75	5.0	5.25	Volts
I_{CC}	@ 5V	—	355	600	mA

MECHANICAL

- Card Dimensions:

Form Factor	H	W	L	Units
STD-Bus	0.60	4.5	6.5	inches

- PC Board thickness: 0.062 inches
- Connectors:
  STD-Bus (J1): 56 pin dual readout; 0.125 inch centers
  SASI Bus (JB): 50 pins; 0.100 inch centers
  Ext. Ready (JA): 2 pin; 0.100 inch centers

ORDERING INFORMATION

Part Number	Description
STD-SASI1	STD-SASI Bus Interface Card
STM-SASI1	STD-SASI1 Technical Manual

COLEX

SASI1

FEATURES

- ☐ STD-Z80 Bus Compatible
- ☐ Supports Shugart Associates Systems Interface (SASI)
- ☐ Auto Handshake Logic
- ☐ Polled or Interrupt Driven
- ☐ I/O Address on 4 Byte Boundary
- ☐ I OEXP Supported
- ☐ 4 MHz Operation
- ☐ Single +5 Volt Supply
- ☐ 1 Year Warranty

DESCRIPTION

STD–SASI1

The Colex STD–SASI1 is designed to interface to the Shugart Associates System Interface™. This interface is designed to allow users at a system level to connect mass storage peripherals without affecting software. The STD–SASI1 implements the host adapter on the STD Bus. This interface is the standard for Winchester 5 1/4 inch disk subsystems. The STD–SASI1 can operate in either a polled or interrupt transfer mode.

The STD–SASI1 consists of two major parts: a parallel data port and status control logic. This port is designed with a 3881 PIO chip. Port A is designated for data and will accept bi-directional information transfers. Port B is designated for status and control. The status signals are inputs; the control signals are outputs from the port. All signals are fully buffered to and from the PIO.

The STD–SASI1 will fully support Z 80 mode 2 interrupts as well as polled operation. The board also has an external connector JA allowing DMA operation. A twisted pair wire can be run from JA to the DMA on board the COLEX STD–FLP2 card. The output signals an external READY output to the DMA which controls a read or write operation. Both commands, data and status may be DMA'd to or from the STD–SASI1.

Automatic handshaking is supported. Jumpet J3 enables a circuit that asserts the SASI ACK (Acknowledge) signal after reading or writing to the SASI Bus. This provides an increase in throughput since software does not have to toggle the ACK control line.

™*Trademark of Shugart Associates*

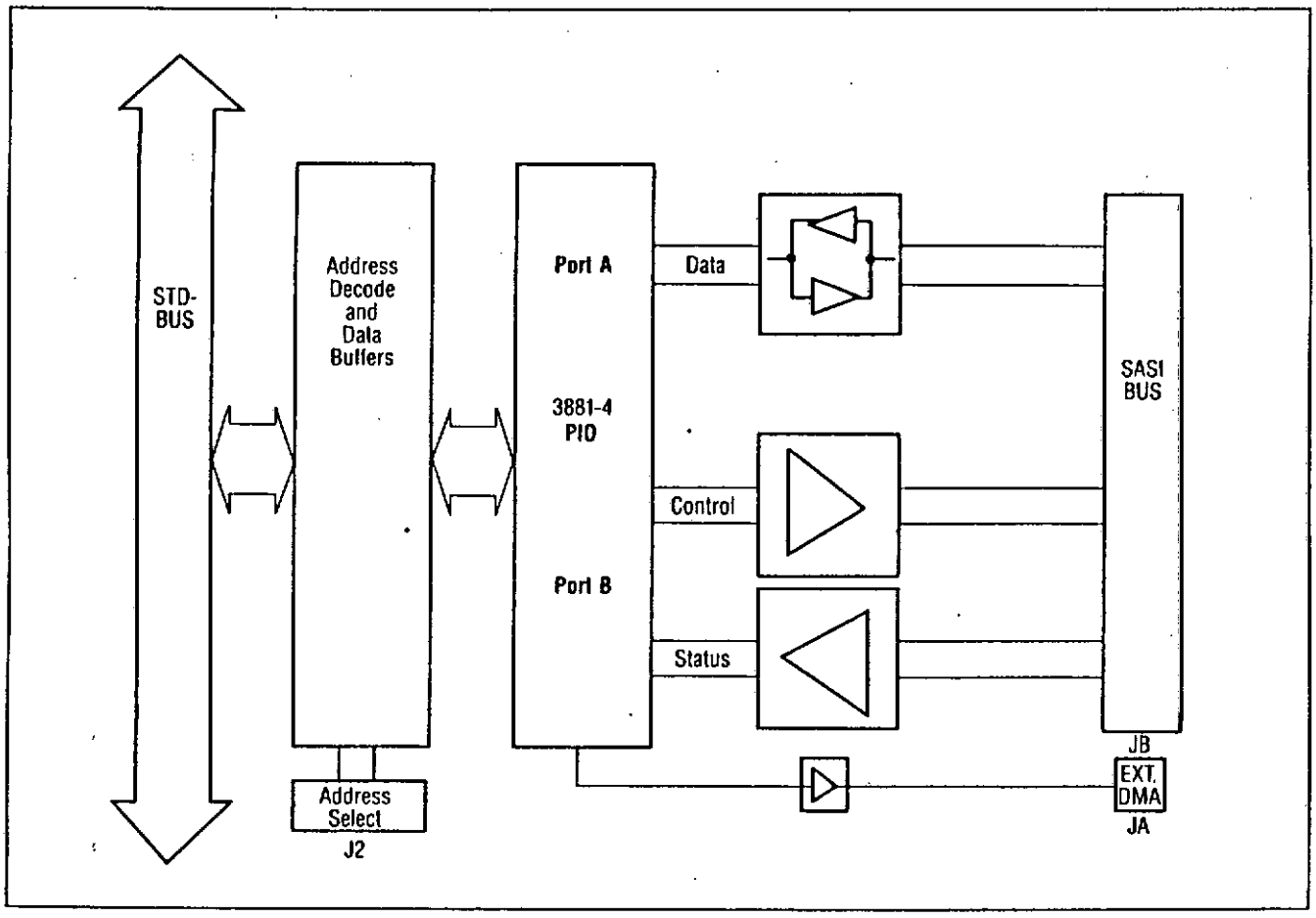


Figure 2. Block Diagram of STD-SASI1

I/O ADDRESSING

The STD-SASI1 is addressed on any 4 byte boundary. The address selection is made using J2 with 6 address lines, A2–A7 and IOEXP. Insertion of a jumper selects a logic zero, no jumper selects a logic 1. For example, to select I/O port 00H, with IOEXP active low, all jumpers must be installed

Address Line	J2 Pin Pairs	Select "0"	Select "1"
A7	13-14	Jumpered	Open
A6	11-12	Jumpered	Open
A5	9-10	Jumpered	Open
A4	7-8	Jumpered	Open
A3	5-6	Jumpered	Open
A2	3-4	Jumpered	Open
!IOEXP	1-2	Jumpered	Open

Figure 3. Address Strapping Options

PORT UTILIZATION

The PIO on-board the STD-SASI1 responds to four sequential port addresses. These four port addresses control data flow, set-up, and interrupt initialization. Below is the base address map for the PIO Data and Control Registers.

A7-A2	A1	A0	Description
X	0	0	Port A Data
X	0	1	Port B Data
X	1	0	Port A Control
X	1	1	Port B Control

Figure 4. Port Utilization

Port A is the bi-directional data port. The data is buffered by bi-directional transceivers connecting the SASI Bus. Port B data is connected to the eight SASI Bus control and status signals. The PIO register designation is as follows:

Port	7	6	5	4	3	2	1	0
A Data	D7	D6	D5	D4	D3	D2	D1	D0
B Data	RES	SEL	ACK	BSY	MSG	C/D	REQ	I/O

Figure 5. SASI Data Port Definition

The Port A and Port B control registers are used for PIO initialization.

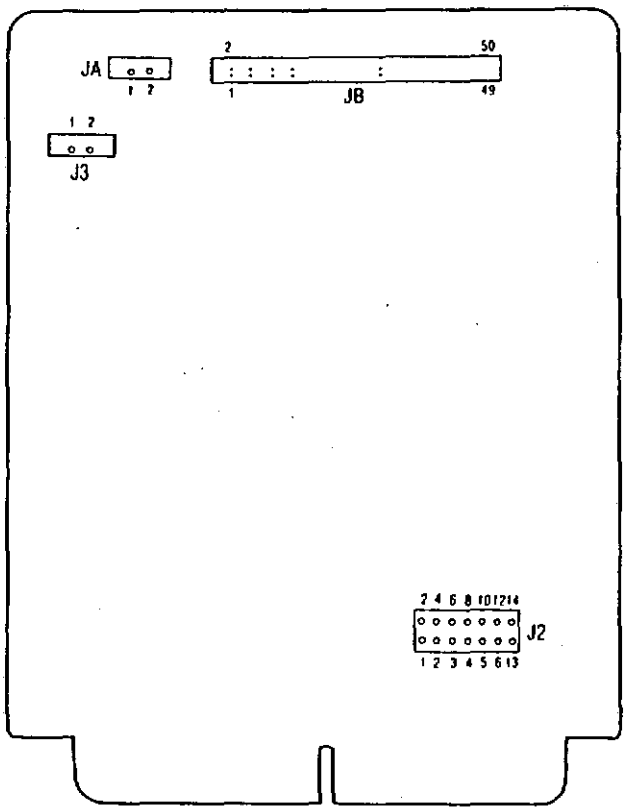


Figure 6. Connectors and Header Locations

HEADER

J1 AUTO ACKNOWLEDGE ENABLE

J1 is the Auto Acknowledge Enable which selects the Auto Acknowledge logic. Insertion of a jumper enables this logic. Typically a system is used with this option enabled.

CONNECTORS

JA EXTERNAL READY OUTPUT

This is an active HIGH signal which may be connected to an external DMA board. External Ready goes HIGH when this REQ (request) signal goes low, which signals that data is available on the SASI Data Bus. Clearing of External Ready occurs by reading from the STD-SASI1 data port. Pin 2 of the connector is an 74LS TTL signal; pin 1 is ground.

JB SASI BUS

Figure 7 shows the symbol, direction and function of the pins of JB, the 50-pin connector for the SASI Bus. The odd pins (1, 3, 5,...) are all grounded, the even pins active or unused. Interconnect is made typically with a 50-pin ribbon cable.

Pin No.	Symbol	Direction	Function
2	DB0	Bi-directional	Data Bit 0
4	DB1	Bi-directional	Data Bit 1
6	DB2	Bi-directional	Data Bit 2
8	DB3	Bi-directional	Data Bit 3
10	DB4	Bi-directional	Data Bit 4
12	DB5	Bi-directional	Data Bit 5
14	DB6	Bi-directional	Data Bit 6
16	DB7	Bi-directional	Data Bit 7
18	N/C	–	–
20	N/C	–	–
22	N/C	–	–
24	N/C	–	–
26	N/C	–	–
28	N/C	–	–
30	N/C	–	–
32	N/C	–	–
34	N/C	–	–
36	BSY	Input	Controller Busy
38	ACK	Output	Request Acknowledge
40	RST	Output	Reset Controller
42	MSG	Input	Complete Message
44	SCL	Output	Select Controller
46	C/D	Input	Command/Data Mode
48	REQ	Input	Request Acknowledge
50	I/O	Input	Data Direction

Figure 7. SASI Bus Signal Definitions

SPECIFICATIONS

- ☐ System clock: 4.0 MHz
- ☐ Data Bus: 8 bits, bi-directional
- ☐ Address Bus: 16 bits
- ☐ Signal Loading: Inputs: One 74LS maximum
  Outputs: I_{OH}=-3mA min @ 2.4 volts
  I_{OL}=24mA @ 0.5 volts
- ☐ Operating Temperature: 0°C to 60°C
- ☐ System Interrupt Units: 1 SIU
- ☐ Interrupts: All three Z80 modes
- ☐ Power Requirements: @ 25° C

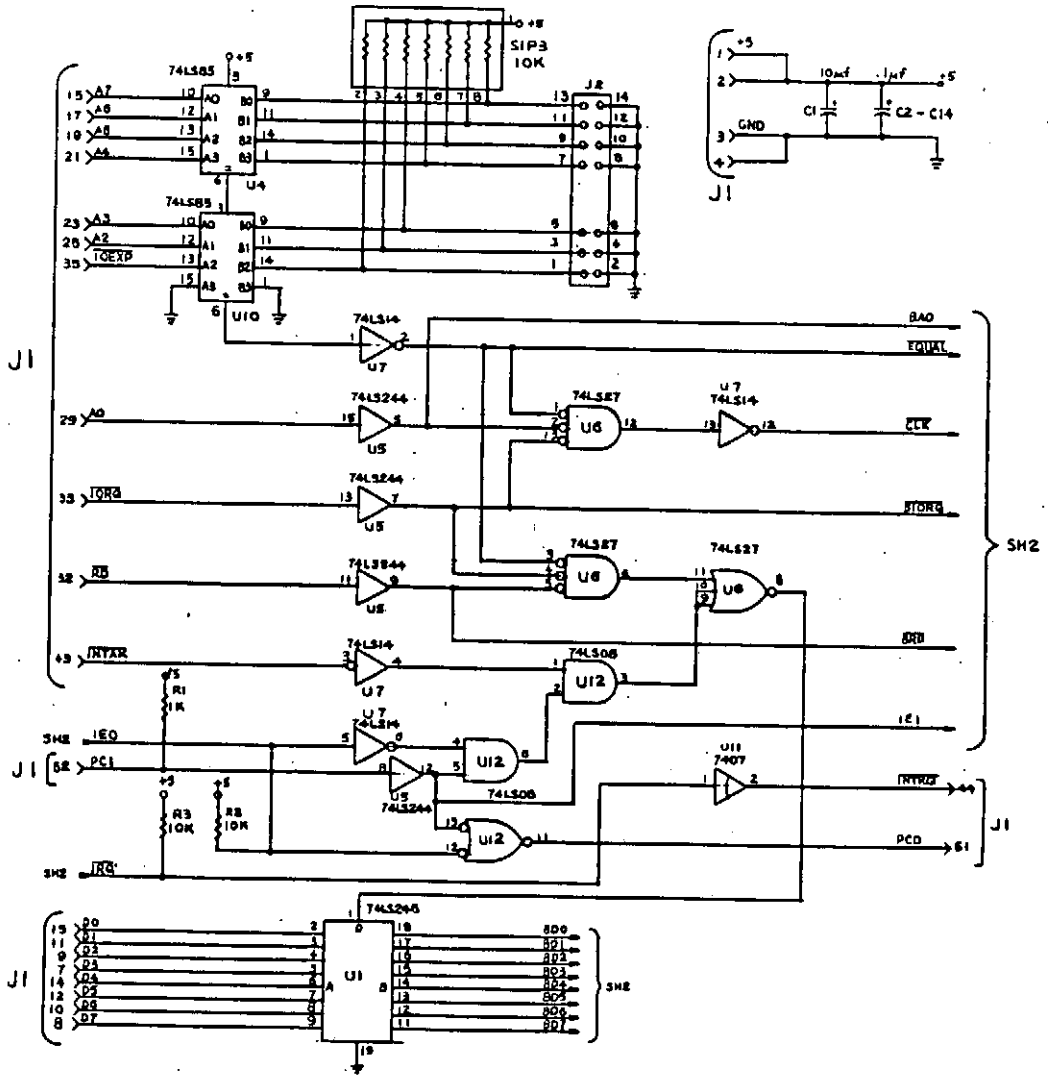
Parameter	Condition	Min.	Typ.	Max.	Units
V_{cc}	—	4.75	5.0	5.25	Volts
I_{cc}	@ 5.0V	–	355	600	mA

MECHANICAL

- ☐ Card Dimensions:

Form Factor	H	W	L	Units
STD-Bus	0.60	4.5	6.5	inches

- ☐ PC Board thickness: 0.062 inches
- ☐ Connectors:
  STD-Bus (J1): 56-pin dual readout; 0.12 inch centers
  SASI Bus (JB): 50 pins; 0.100 inch centers
  Ext. Ready (JA): 2-pin; 0.100 inch centers

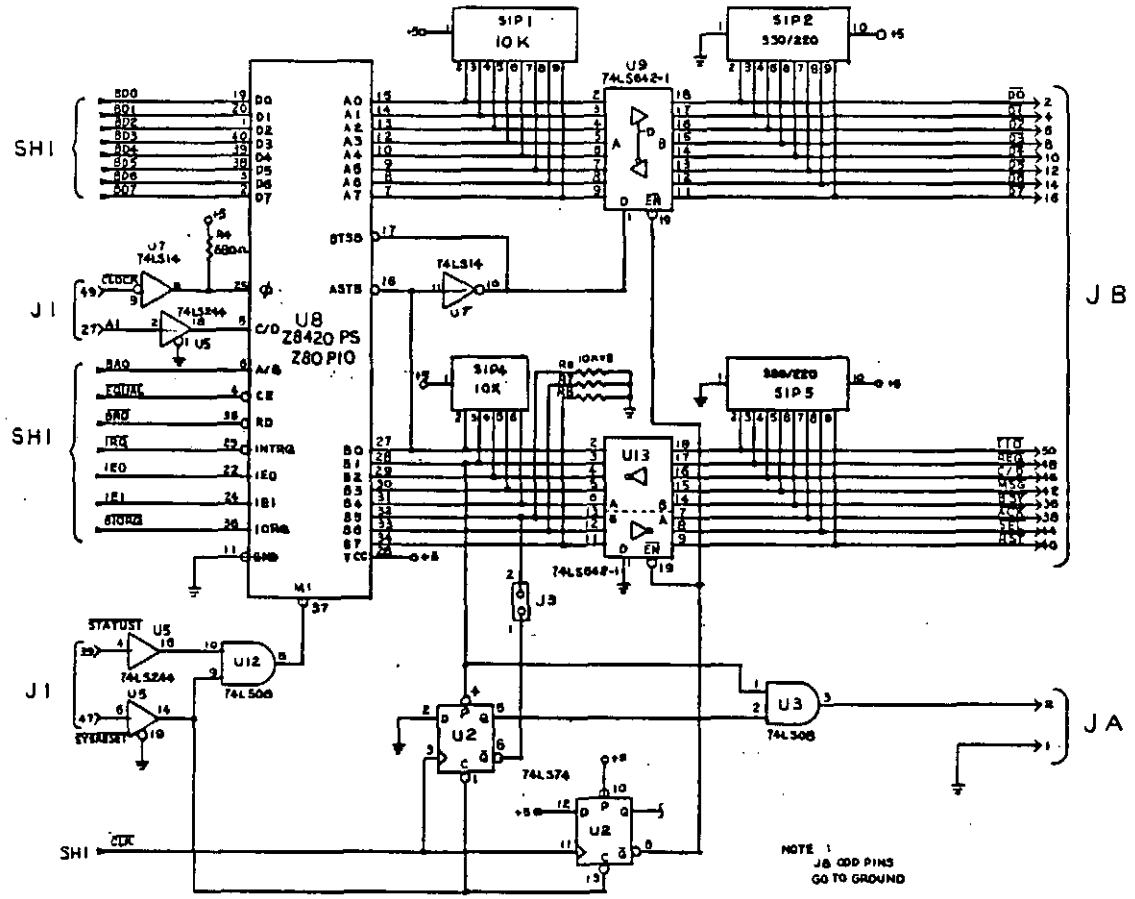


REV.	DATE	REVISION RECORD	ECN #

COLEX ELECTRONIC CO., LTD.

TITLE: STD-SASI I

DRAWN	DATE	DRAWING NO. 07-06-001 REV.A
CHECKED	DATE	PROJECT/NEXT ASSY. NO. 09-05-000
APPROVED	DATE	SCALE / SHEET 1 OF 2



REV.	DATE	REVISION RECORD	ECN #

COLEX ELECTRONICS CO., LTD.

TITLE: STD-SASI 1

DRAWN	DATE 08/17/83	DRAWING NO.	07-06-001 REVA
CHECKED	DATE	PROJECT/NEXT ASSY. NO.	09-06-000
APPROVED	DATE	SCALE	SHEET 1 OF 2